**Title**: **Design and Verification of SRAM using System Verilog**.

**Abstract**: This System Verilog verification project aims to verify the functionality, timing, and working of Static Random Access Memory (SRAM) . Utilizing SystemVerilog's capabilities, the project follows a structured approach with testbenches , random stimulated generators, drivers and monitor files. The project aims to verify SRAM designs efficiently under various operating conditions demonstrating its reliability through generated testbenches.

**Uses of SRAM**:

1.SRAM plays a crucial role in microprocessors and microcontrollers as primary memory, ensuring fast access times and low latency, thereby enhancing overall system performance.

2.In embedded systems and networking devices, SRAM is utilized in cache memories to store frequently accessed data, optimizing system performance by reducing access times to critical information.

**Expected outcomes:**

* **Performance Validation**: The project will verify that the SRAM design operates as intended, meeting the speed and efficiency requirements. This is similar to checking if a new sports car can reach its advertised top speed on the track; the project ensures that the SRAM performs as fast and efficiently as it should in real-world scenarios.
* **Reliability Assurance**: By conducting various tests and simulations, the project will ensure that the SRAM design is dependable and can be trusted to store and retrieve data accurately over time. It's like ensuring that a safe you use to keep your valuables will reliably lock and unlock every time you need it, without any surprises or malfunctions.